

<Intelligent Power Modules>

PM50CG1B120

FLAT-BASE TYPE
INSULATED PACKAGE



FEATURE

- a) Adopting Full-Gate CSTBT™ chip.
- b) The over-temperature protection which detects the chip surface temperature of CSTBT™ is adopted.
- c) Error output signal is available from each protection upper and lower arm of IPM.
- d) Outputting an error signal corresponding to the abnormal state (error mode identification)

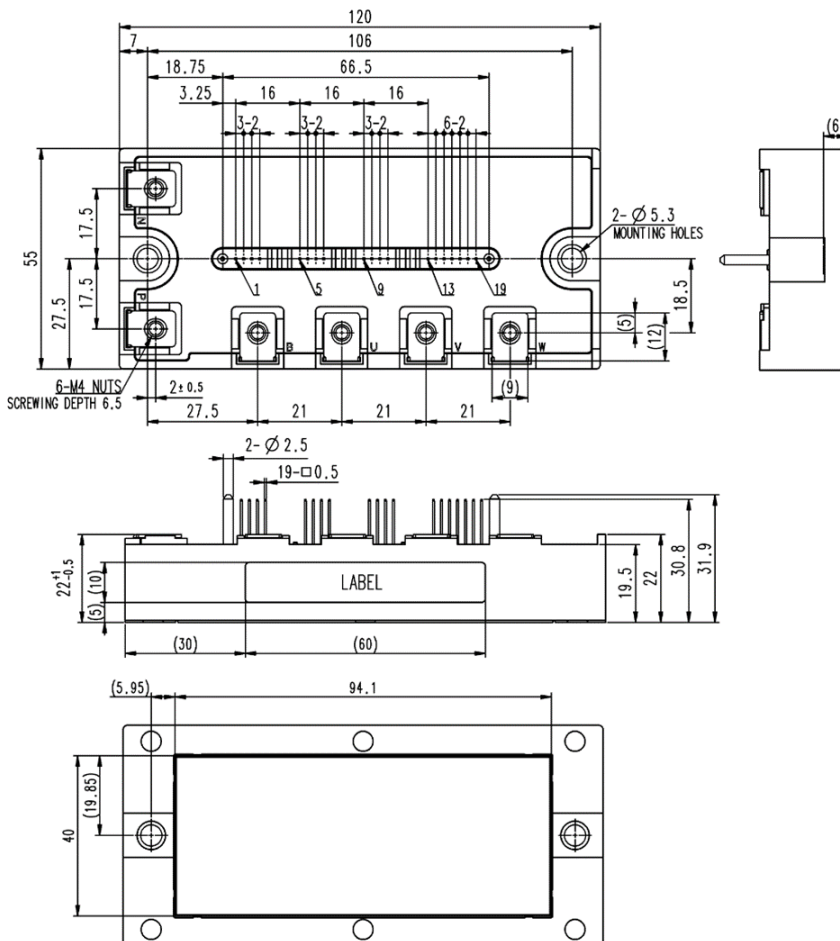
UL Recognized under UL1557, File No. E323585

This product is compliant with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive 2011/65/EU.

APPLICATION

General purpose inverter, servo drives and other motor controls

PACKAGE OUTLINES



Dimensions in mm

Tolerance otherwise specified

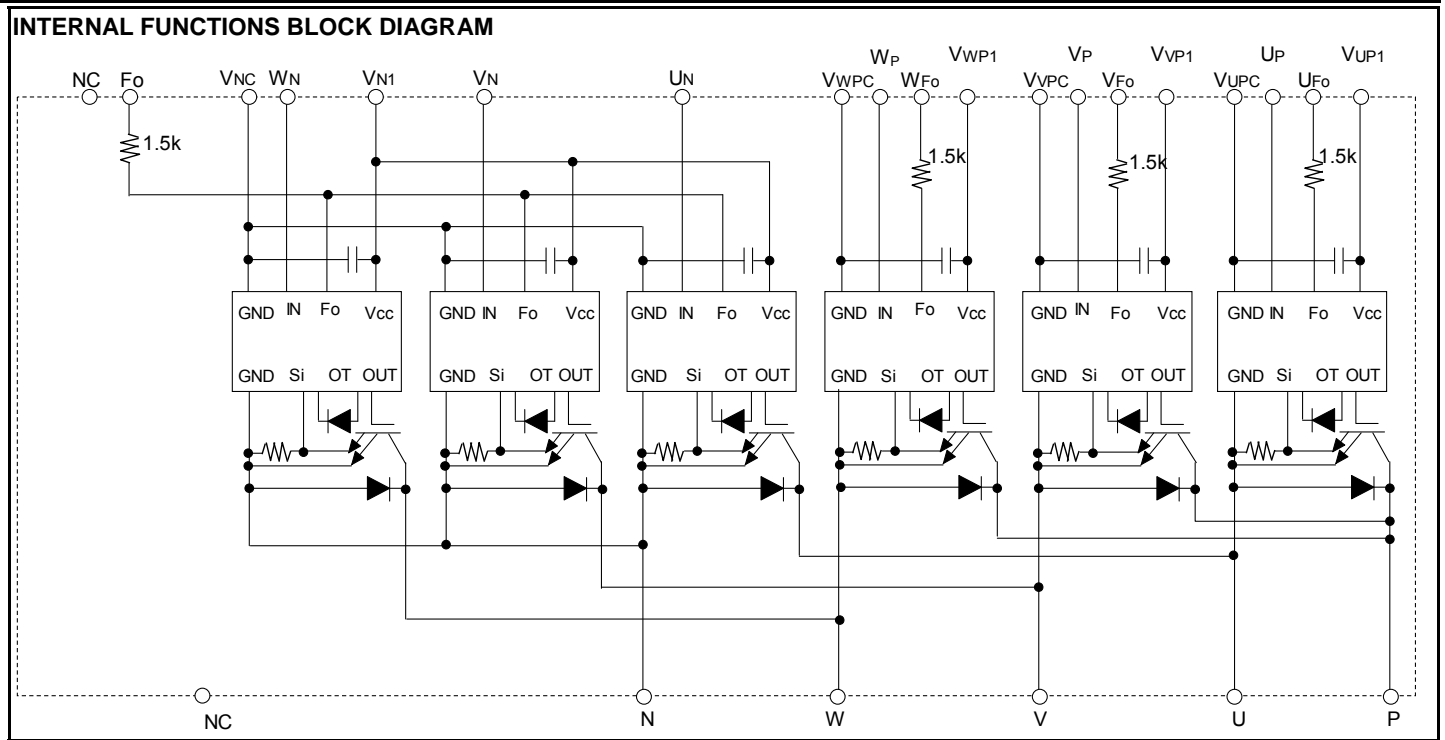
Division of Dimension		Tolerance
0.5	to 3	±0.2
over 3	to 6	±0.3
over 6	to 30	±0.5
over 30	to 120	±0.8
over 120	to 400	±1.2

TERMINAL CODE

1. V_{UPC}
2. U_{FO}
3. U_P
4. V_{UP1}
5. V_{VPC}
6. V_{FO}
7. V_P
8. V_{VP1}
9. V_{WPC}
10. W_{FO}
11. W_P
12. V_{WP1}
13. V_{NC}
14. V_{N1}
15. NC
16. U_N
17. V_N
18. W_N
19. F_O

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HIGH POWER SWITCHING USE
INSULATED TYPE



MAXIMUM RATINGS (T_{vj} = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Conditions	Ratings	Unit
V _{CES}	Collector-Emitter Voltage	V _D =15 V, V _{CIN} =15 V	1200	V
I _C	Collector Current	T _C =25 °C	50	A
I _{CRM}		Pulse	100	
P _{tot}	Total Power Dissipation	T _C =25 °C	378	W
I _E	Emitter Current (Free-wheeling Diode Forward current)	T _C =25 °C	50	A
I _{ERM}		Pulse	100	
T _{vj}	Junction Temperature		-20 ~ +150	°C

*: T_c measurement point is just under the chip.

CONTROL PART

Symbol	Parameter	Conditions	Ratings	Unit
V _D	Supply Voltage	Applied between: V _{UP1} -V _{UPC} , V _{VP1} -V _{VPC} , V _{WP1} -V _{WPC} , V _{N1} -V _{NC}	20	V
V _{CIN}	Input Voltage	Applied between: U _P -V _{UPC} , V _P -V _{VPC} , W _P -V _{WPC} , U _N , V _N , W _N -V _{NC}	20	V
V _{FO}	Fault Output Supply Voltage	Applied between: U _{FO} -V _{UPC} , V _{FO} -V _{VPC} , W _{FO} -V _{WPC} , F _O -V _{NC}	20	V
I _{FO}	Fault Output Current	Sink current at U _{FO} , V _{FO} , W _{FO} , F _O terminals	20	mA

TOTAL SYSTEM

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC(PROT)}	Supply Voltage Protected by SC	V _D =13.5 V~16.5 V, Inverter Part, T _{vj} =+125°C start	800	V
T _{stg}	Storage Temperature	-	-40 ~ +125	°C
T _C	Operating Case Temperature	-	-20 ~ +125	°C
V _{isol}	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base plate, AC 1min, RMS	2500	V

*: T_c measurement point is just under the chip.

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HIGH POWER SWITCHING USE
INSULATED TYPE

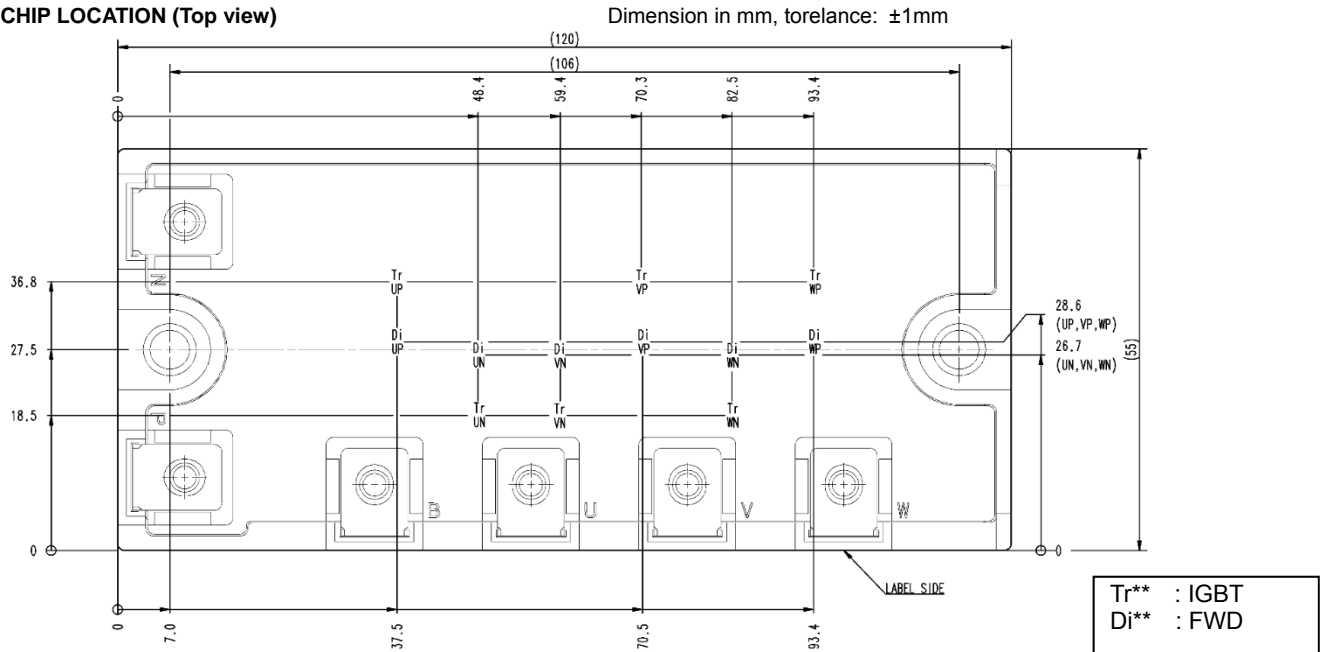
THERMAL RESISTANCE

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Thermal Resistance	Junction to case, IGBT, per 1 element (Note1)	-	-	0.33	K/W
$R_{th(j-c)D}$		Junction to case, FWD, per 1 element (Note1)	-	-	0.51	
$R_{th(c-s)}$	Contact Thermal Resistance	Case to heat sink, per 1 module, Thermal grease applied (Note.1, 2)	-	14.4	-	K/kW

Note1. If you use this value, $R_{th(s-a)}$ should be measured just under the chips.

Note2. Typical value is measured by using thermally conductive grease of $\lambda=0.9W/(m\cdot K)$, $D_{(c-s)}=50\ \mu m$.

CHIP LOCATION (Top view)



ELECTRICAL CHARACTERISTICS ($T_{vj}=25^{\circ}C$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Conditions	Limits			Unit		
			Min.	Typ.	Max.			
V_{CESat}	Collector-Emitter Saturation Voltage	$V_D=15\ V, I_C=50\ A$ $V_{CIN}=0\ V$, Pulsed, (Fig.1)	$T_{vj}=25^{\circ}C$	Terminal	-	-	1.75	V
			Chip	-	1.3	-		
		$T_{vj}=125^{\circ}C$	Terminal	-	-	2.0		
			Chip	-	1.5	-		
V_{EC}	Emitter-Collector Voltage	$V_D=15\ V, I_E=50\ A$, $V_{CIN}=15\ V$, pulsed, (Fig.2)	$T_{vj}=25^{\circ}C$	Terminal	-	-	2.35	V
			Chip	-	1.75	-		
		$T_{vj}=125^{\circ}C$	Terminal	-	-	2.6		
			Chip	-	1.95	-		
t_{on}	Switching Time	$V_D=15\ V, V_{CIN}=0\ V \leftrightarrow 15\ V$, $V_{CC}=600\ V, I_C=50A$, $T_{vj}=125^{\circ}C$, Inductive Load (Fig.3, 4)		0.3	0.7	1.2	μs	
t_{rr}				-	0.13	0.4		
$t_{c(on)}$				-	0.2	0.4		
t_{off}				-	1.0	2.8		
$t_{c(off)}$				-	0.4	1.2		
I_{CES}	Collector-Emitter Cut-off Current	$V_{CE}=V_{CES}, V_D=15\ V$, $V_{CIN}=15\ V$ (Fig.5)	$T_{vj}=25^{\circ}C$	-	-	1	mA	
			$T_{vj}=125^{\circ}C$	-	-	10		

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ELECTRICAL CHARACTERISTICS (Tvj = 25°C, unless otherwise noted)

CONTROL PART

Symbol	Parameter	Conditions	Limits			Unit	
			Min.	Typ.	Max.		
I _D	Circuit Current	V _D =15 V, V _{CIN} =15 V	V _{P1} -V _{PC}	-	4	6	mA
			V _{N1} -V _{NC}	-	12	18	
		V _D =15 V, V _{CIN} =0 V ↔ 15 V, V _{CC} =800 V I _C =0A, Tvj=125 °C, f _C ≤20kHz	V _{P1} -V _{PC}	-	16	20	
			V _{N1} -V _{NC}	-	49	59	
V _{th(ON)}	Input ON Threshold Voltage	Applied between:	1.2	1.5	1.8	V	
V _{th(OFF)}	Input OFF Threshold Voltage	U _P -V _{UPC} , V _P -V _{VPC} , W _P -V _{WPC} , U _N , V _N , W _N -V _{NC}	1.7	2.0	2.3		
SC	Short Circuit Trip Level	-20≤Tvj≤125 °C, V _D =15 V (Fig.3, 6)	100	-	-	A	
t _{d(SC)}	Short Circuit Current Delay Time	V _D =15 V, Tvj=125 °C (Fig.3, 6)	-	2.0	-	μs	
OT	Over Temperature Protection	Detect temperature of IGBT chip surface	Trip level	150	-	-	°C
OT _(hys)			Hysteresis	-	20	-	
UV _t	Supply Circuit	-	Trip level	11.0	12.0	12.7	V
UV _r	Under-Voltage Protection		Reset level	-	12.5	-	
I _{FO(H)}	Fault Output Current	V _D =15 V, V _{FO} =15 V (Note3)	-	-	0.01	mA	
I _{FO(L)}			-	10	15		
t _{FO}	Fault Output Pulse Width	V _D =15 V (Note3)	OT	-	8.0	-	ms
			UV	-	4.0	-	
			SC	-	2.0	-	

Note3. Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

MECHANICAL RATINGS AND CHARACTERISTICS

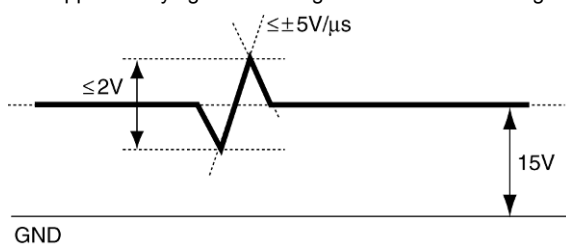
Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
M _s	Mounting Torque	Mounting part screw : M5	2.5	3.0	3.5	N•m
M _t	Mounting Torque	Main terminal part screw : M4	1.5	1.7	2.0	
m	mass	-	-	260	-	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Conditions	Recommended value	Unit
V _{CC}	Supply Voltage	Applied across P-N terminals	≤ 800	V
V _D	Control Supply Voltage	Applied between : V _{UP1} -V _{UPC} , V _{VP1} -V _{VPC} , V _{WP1} -V _{WPC} , V _{N1} -V _{NC} (Note4)	15.0±1.5	V
V _{CIN(ON)}	Input ON Voltage	Applied between : U _P -V _{UPC} , V _P -V _{VPC} , W _P -V _{WPC} , U _N , V _N , W _N -V _{NC}	≤ 0.8	V
V _{CIN(OFF)}	Input OFF Voltage		≥ 9.0	
f _{PWM}	PWM Input Frequency	Using Application Circuit of Fig. 8	≤ 20	kHz
t _{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig.7)	≥ 2.5	μs

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Note4. With ripple satisfying the following conditions: dv/dt swing ≤ ±5 V/μs, Variation ≤ 2 V peak to peak



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PRECAUTIONS FOR TESTING

1. Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.

After this, the specified ON and OFF level setting for each input signal should be done.

2. When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.

(These test should not be done by using a curve tracer or its equivalent.)

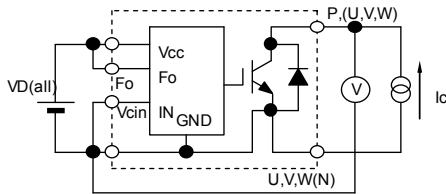


Fig.1 V_{CESat} Test



Fig.2 V_{EC} Test

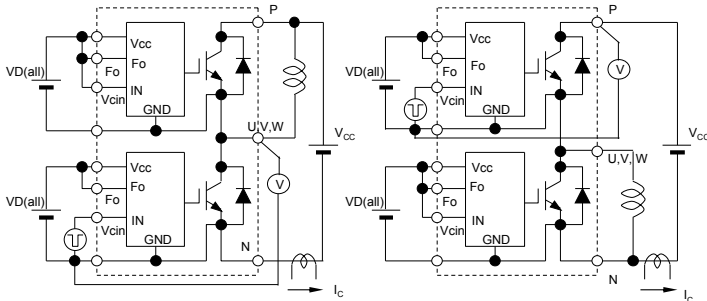


Fig.3 Switching time and SC test circuit

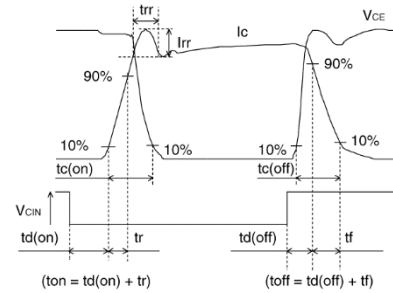


Fig.4 Switching time test waveform

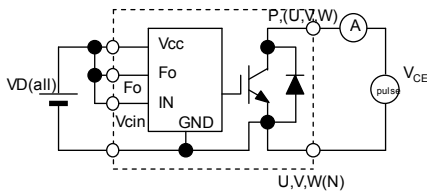


Fig.5 I_{CES} Test

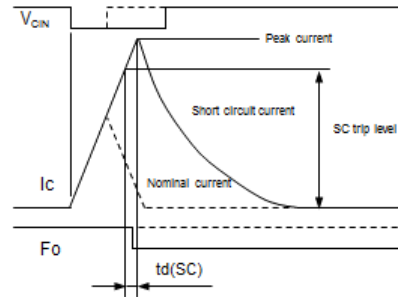
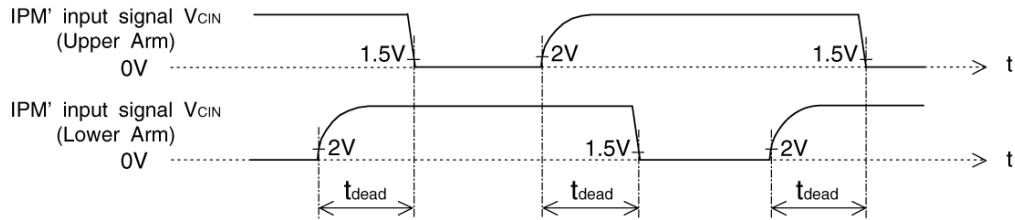


Fig.6 SC test waveform



1.5V: Input on threshold voltage $V_{th(on)}$ typical value, 2V: Input off threshold voltage $V_{th(off)}$ typical value

Fig. 7 Dead time measurement point example

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Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

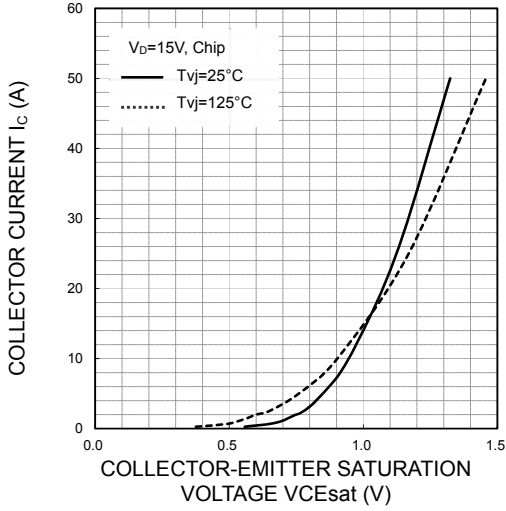
- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers: $t_{PLH}, t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler: CTR > 100%
- Use 4 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.

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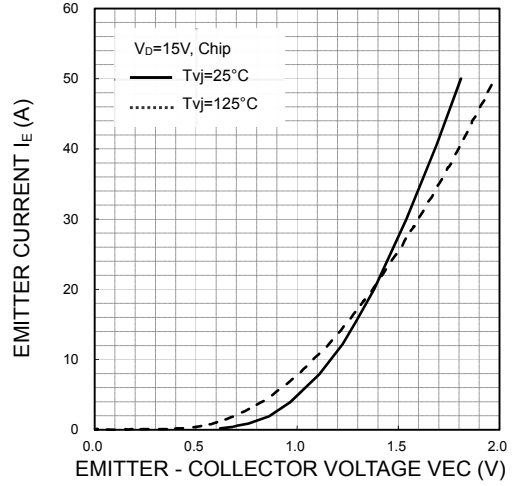
HIGH POWER SWITCHING USE
INSULATED TYPE

PERFORMANCE CURVES

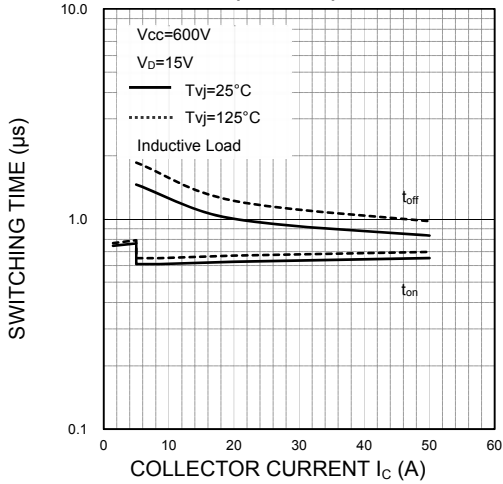
COLLECTOR-EMITTER SATURATION VOLTAGE (VS. I_C) CHARACTERISTICS (TYPICAL)



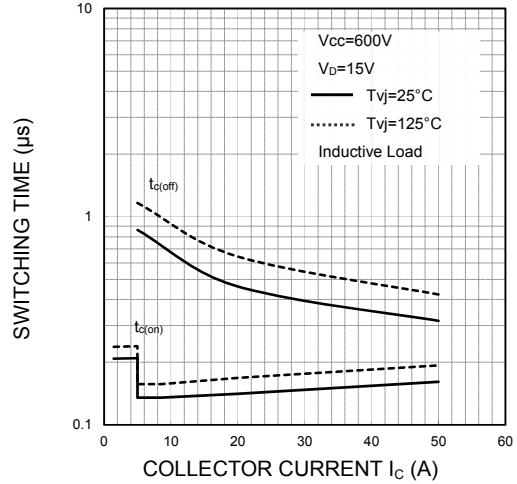
FREE WHEELING DIODE FORWARD CHARACTERISTICS (TYPICAL)



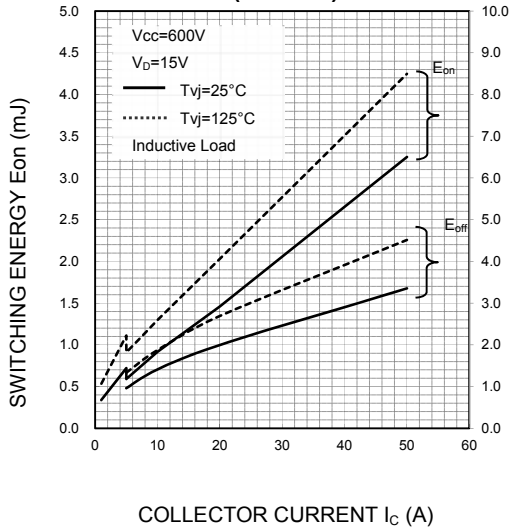
SWITCHING TIME (t_{on} , t_{off}) CHARACTERISTICS (TYPICAL)



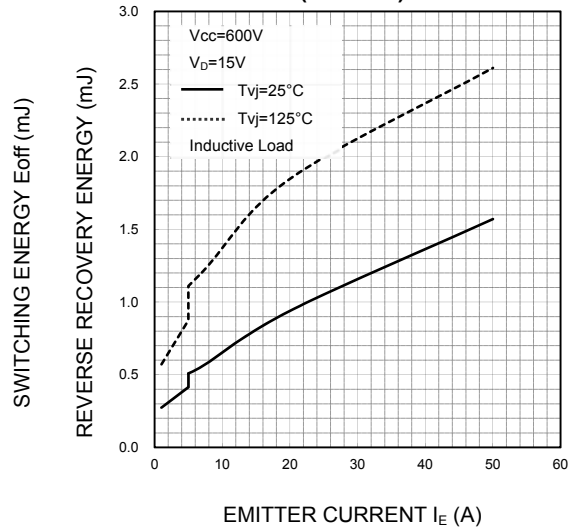
SWITCHING TIME ($t_{c(on)}$, $t_{c(off)}$) CHARACTERISTICS (TYPICAL)



SWITCHING ENERGY CHARACTERISTICS (TYPICAL)



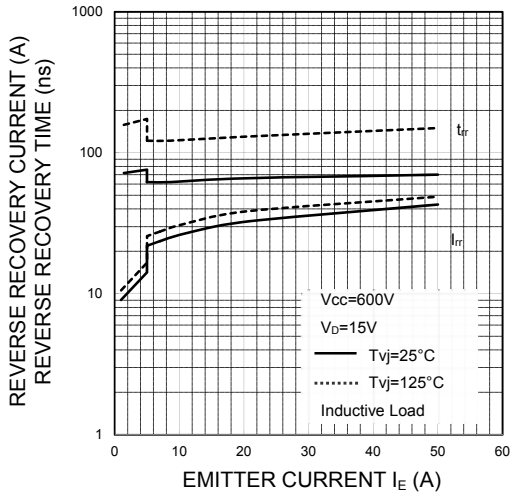
FREE WHEELING DIODE REVERSE RECOVERY ENERGY CHARACTERISTICS (TYPICAL)



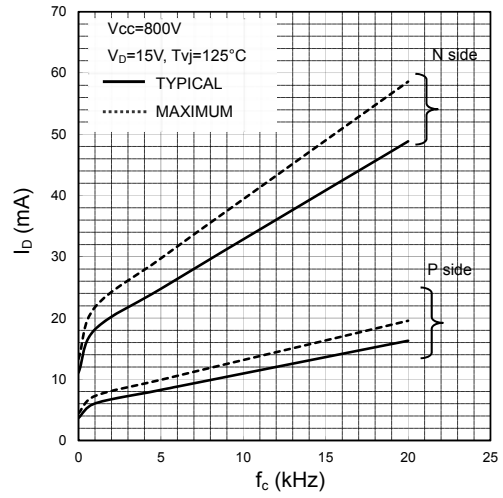
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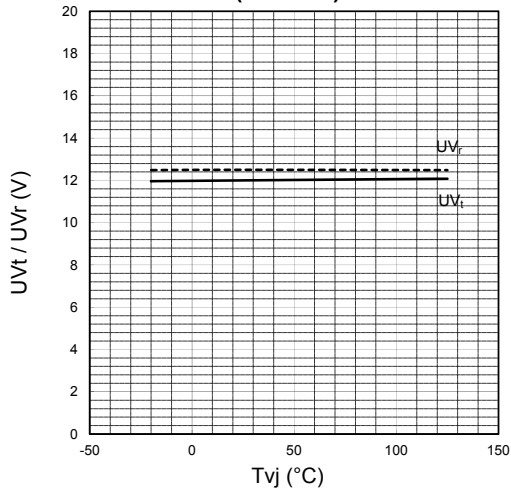
FREE WHEELING DIODE REVERSE RECOVERY CHARACTERISTICS (TYPICAL)



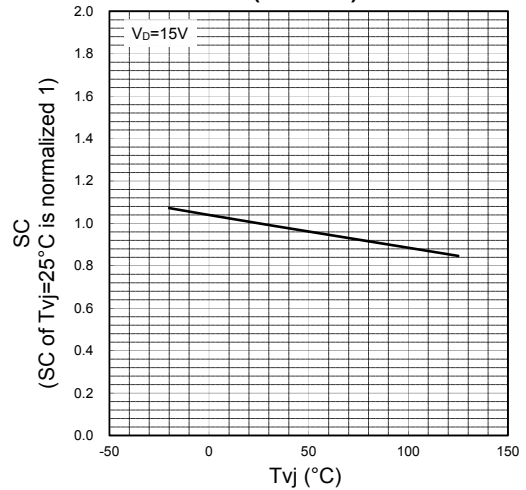
I_D VS. f_c CHARACTERISTICS (TYPICAL, MAXIMUM)



UV TRIP LEVEL VS. T_{vj} CHARACTERISTICS (TYPICAL)

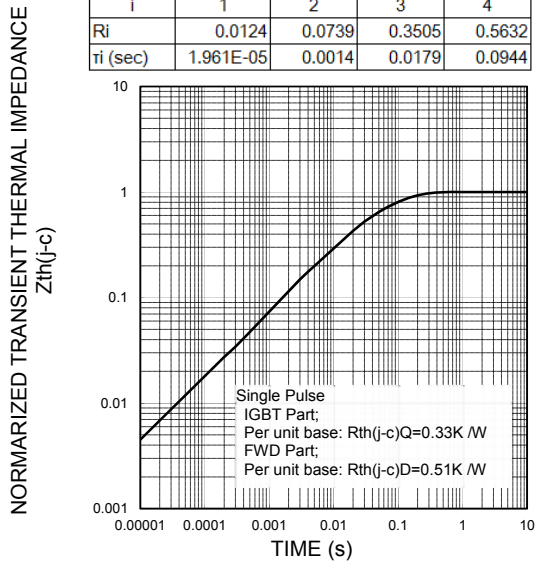


SC TRIP LEVEL VS. T_{vj} CHARACTERISTICS (TYPICAL)



TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (TYPICAL)

i	1	2	3	4
R_{ti}	0.0124	0.0739	0.3505	0.5632
t_i (sec)	1.961E-05	0.0014	0.0179	0.0944



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