2SD300C17Ax Preliminary Datasheet

Dual-Channel High-quality and Low-cost SCALE-2 Driver Core

Abstract

The SCALE-2 dual-driver core 2SD300C17Ax is a second source to Infineon's 2ED300C17-S and 2ED300C17-ST. The driver is fully pin and function-compatible to the 2ED300C17-S/2ED300C17-ST and was designed for applications in which high reliability is expected.

The use of CONCEPT's highly integrated SCALE-2 chipset allows 63% of the components to be dispensed with compared to the 2ED300C17-S/2ED300C17-ST. This advantage is impressively reflected in increased reliability (function and MTBF) with simultaneously lower costs.

The 2SD300C17Ax combines a complete two-channel driver core with all components required for driving, such as an isolated DC/DC converter, short-circuit protection, failure soft shut down, short pulse suppression as well as supply voltage monitoring. Each of the two output channels is electrically isolated from the primary side and the other secondary channel.

The driver provides a gate voltage swing of ±15V. An output current of 30A and 4W drive power is available per channel.

Its outstanding EMC with a dv/dt strength of more than 50V/ns allows safe and reliable operation in even the demanding industrial applications

Product Highlights

- ✓ Dual channel driver
- ✓ Highly integrated SCALE-2 chipset
- ✓ Switching frequency up to 60kHz
- ✓ Gate current ±30A
- ✓ 4W output power per channel
- ✓ Direct and half-bridge mode
- ✓ IGBT short-circuit protection
- ✓ Failure soft shut down
- ✓ Isolated DC/DC converter
- ✓ Safe isolation to EN 50178
- ✓ UL compliant
- ✓ Reliable, long service life
- ✓ Coated version also available

Applications

- ✓ 1:1 replacement of 2ED300C17-S
- ✓ 1:1 replacement of 2ED300C17-ST
- ✓ IGBTs up to 1700V

Preliminary Data Sheet

Safety Notice!

The data contained in this data sheet is intended exclusively for technically trained staff. Handling all high-voltage equipment involves risk to life. Strict compliance with the respective safety regulations is mandatory!

Any handling of electronic devices is subject to the general specifications for protecting electrostatic-sensitive devices according to international standard IEC 60747-1, Chapter IX or European standard EN 100015 (i.e. the workplace, tools, etc. must comply with these standards). Otherwise, this product may be damaged.

Important Product Documentation

This data sheet contains only product-specific data. For a detailed description, must-read application notes and important information that apply to this product, please refer to "2SD300C17 Description & Application Manual" on www.igbt-driver.com/go/2SD300C17

Absolute Maximum Ratings

Parameter	Remarks	Min	Max	Unit
Supply voltage V_{DC}	VDC to GND	0	16	V
Supply voltage V_{DD}	VDD to GND	0	16	V
Logic input voltages	INA, INB and Mod to GND	-0.5	20	V
Logic output voltages	SOA and SOB to GND	-0.5	VDD+0.5	V
SOx current	Failure condition, total current		20	mA
Gate peak current I_{out}	Note 1	-30	+30	A
Gate resistance	Turn-on and turn-off	1		Ω
IGBT gate charge			50	µC
Average supply current I_{DC}	Notes 2, 3		540	mA
Output power	Ambient temperature <70°C (Notes 4, 5)		4	W
	Ambient temperature 85°C (Note 4)		3	W
Switching frequency F			60	kHz
Test voltage (50Hz/1min.)	Primary to secondary (Note 13)		5000	$V_{AC(eff)}$
	Secondary to secondary (Note 13)		4000	$V_{AC(eff)}$
|dV/dt|	Rate of change of input to output voltage (Note 6)		50	kV/µs
Operating voltage	Primary and secondary to secondary side		1700	V_{peak}
Operating temperature	Note 5	-40	+85	°C
Storage temperature		-40	+90	°C

Recommended Operating Conditions

Power Supply	Remarks	Min	Typ	Max	Unit
Supply voltage V_{DC}	VDC to GND	14	15	16	V
Supply voltage V_{DD}	VDD to GND	14	15	16	V
Input logic level	INx and Mod to GND, high level		VDD		V
Input logic level	INx and Mod to GND, low level		0		V

Electrical Characteristics

All data refer to +25°C and V_{DC} = V_{DD} = 15V unless otherwise specified.

Power supply	Remarks	Min	Typ	Max	Unit
Supply current I_{DC}	Without load		65		mA
Supply current I_{DD}	Direct mode, F = 0Hz		14		mA
Supply current I_{DD}	Direct mode, F = 60kHz		21		mA
Coupling capacitance C_{io}	Primary to secondary, per channel		31		pF
	Secondary to secondary		29		pF
Power Supply Monitoring	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Supply threshold V_{DD}	Primary side, clear fault	11.9	12.6	13.3	V
	Primary side, set fault (Note 7)	11.3	12.0	12.7	V
Monitoring hysteresis	Primary side, set/clear fault	0.35			V
Supply threshold V_{x+}-V_{COMx}	Secondary side, clear fault	12.1	12.6	13.1	V
	Secondary side, set fault (Note 8)	11.5	12.0	12.5	V
Monitoring hysteresis	Secondary side, set/clear fault	0.35			V
Supply threshold V_{COMx}-V_{x-}	Secondary side, clear fault	5	5.15	5.3	V
	Secondary side, set fault (Note 8)	4.7	4.85	5	V
Monitoring hysteresis	Secondary side, set/clear fault	0.15			V
Logic Inputs and Outputs	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Input impedance	INx and Mod		3.9		kΩ
Turn-on threshold	V(INx)		8.1		V
Turn-off threshold	V(INx)		4.8		V
SOx output voltage	Failure condition, I(SOx)<20mA			0.7	V
Short-Circuit Protection	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Rth value	Between RCx and COM x	2		70	kΩ
Blocking time	Note 12		27		ms

External Fault input	Remarks	Min	Typ	Max	Unit
Threshold level	Between E.x and COM x		5		V
Timing Characteristics	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Turn-on delay $t_{d(on)}$	Direct mode (Note 9)		630		ns
Turn-off delay $t_{d(off)}$	Direct mode (Note 9)		490		ns
Short pulse suppression	Turn-on command pulse width		470		ns
	Turn-off command pulse width		300		ns
Dead time between channels	Half-bridge mode, with CA=CB=0pF (Note 15)		1.3		µs
Transmission delay of fault state	Note 10		450		ns
Output Voltage	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Turn-on voltage	Gate x to COM x		15		V
Turn-off voltage	Gate x to COM x		-15		V
Electrical Isolation	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Test voltage (50Hz/1s)	Primary to secondary side (Note 13)	5000	5050	5100	V_{eff}
	Secondary to secondary side (Note 13)	4000	4050	4100	V_{eff}
Partial discharge extinction volt.	Primary to secondary side (Note 14)	1768			V_{peak}
	Secondary to secondary side (Note 14)	1700			V_{peak}
Creepage distance	Primary to secondary side	16.2			mm
	Secondary to secondary side	14.2			mm
Clearance distance	Primary to secondary side	16.2			mm
	Secondary to secondary side	6.5			mm
Output	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Blocking capacitance	Vx+ to COMx		9.4		µF
	COMx to Vx-		9.4		µF

Footnotes to the Key Data

1) The maximum peak gate current refers to the highest current level occurring during the product lifetime. It is an absolute value and does also apply for short pulses.
2) The average supply input current is limited for thermal reasons. Higher values than specified by the absolute maximum rating are permissible (e.g. during power supply start up) if the average remains below the given value, provided the average is taken over a time period which is shorter than the thermal time constants of the driver in the application.
3) There is no means of actively controlling or limiting the input current in the driver. In the case of start-up with very high blocking capacitor values, or in case of short circuit at the output, the supply input current has to be limited externally.
4) The maximum output power must not be exceeded at any time during operation. The absolute maximum rating must also be observed for time periods shorter than the thermal time constants of the driver in the application.
5) An extended output power range is specified for maximum ambient temperatures of 70°C.

6) This specification guarantees that the drive information will be transferred reliably even at a high DC-link voltage and with ultra-fast switching operations.
7) Undervoltage monitoring of the primary-side supply voltage (V_{DD} to GND). If the voltage drops below this limit, a fault is transmitted to both outputs SOA and SOB and the IGBTs are switched off.
8) Undervoltage monitoring of the secondary-side supply voltage (Vx+ to COMx and COMx to Vx- which correspond with the approximate turn-on and turn-off gate-emitter voltages). If the corresponding voltage drops below this limit, the IGBT is switched off and a fault is transmitted to the corresponding SOx output on the primary side.
9) The delay time is measured between 50% of the input signal and 10% (turn-on) or 90% (turn-off) of the corresponding output.
10) Transmission delay of fault state from the secondary side to the primary status output.
11) The test voltage of $4000V_{AC(eff)}$/50Hz may be applied only once during one minute. It should be noted that with this (strictly speaking obsolete) test method, some (minor) damage occurs to the insulation layers due to the partial discharge. Consequently, this test is not performed at CONCEPT as a series test. In the case of repeated isolation tests (e.g. module test, equipment test, system test), the subsequent tests should be performed with a lower test voltage: the test voltage is reduced by 400V for each additional test. The more modern if more elaborate partial-discharge measurement is preferable to such test methods as it is almost entirely non-destructive.
12) The blocking time sets a minimum time span between the end of any fault state and the start of normal operation (remove fault from pin SOx). The value of the blocking time is programmed on the driver and cannot be modified externally.
13) HiPot testing (= dielectric testing) must generally be restricted to suitable components. This gate driver is suited for HiPot testing. Nevertheless, it is strongly recommended to limit the testing time to 1s slots as stipulated by EN 50178. Excessive HiPot testing at voltages much higher than $1200V_{AC(eff)}$ may lead to insulation degradation. No degradation has been observed over 1min. testing at $5000V_{AC(eff)}$. Every production sample shipped to customers has undergone 100% testing at the given value for 1s.
14) Partial discharge measurement is performed in accordance with IEC 60270 and isolation coordination specified in EN 50178. The partial discharge extinction voltage between primary and either secondary side is coordinated for safe isolation to EN 50178.
15) The dead time is measured between 50% voltage swing of the gate-emitter voltage which is turned off and 50% voltage swing of the gate-emitter voltage which is turned-on.

Legal Disclaimer

This data sheet specifies devices but cannot promise to deliver any specific characteristics. No warranty or guarantee is given – either expressly or implicitly – regarding delivery, performance or suitability.

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Ordering Information

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Type Designation	Description
2SD300C17A0	Dual-channel SCALE-2 driver core (uncoated)
2SD300C17A0-T	Dual-channel SCALE-2 driver core (coated with varnish)

Product home page: www.IGBT-Driver.com/go/2SD300C17

Refer to www.IGBT-Driver.com/go/nomenclature for information on driver nomenclature

Information about Other Products

For other drivers, product documentation, and application support

Please click: www.IGBT-Driver.com

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