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PHASE CONTROL THYRISTOR

AT631LT

Repetitive voltage up to **1800 V**
Mean forward current **4477 A**
Surge current **65 kA**

FINAL SPECIFICATION

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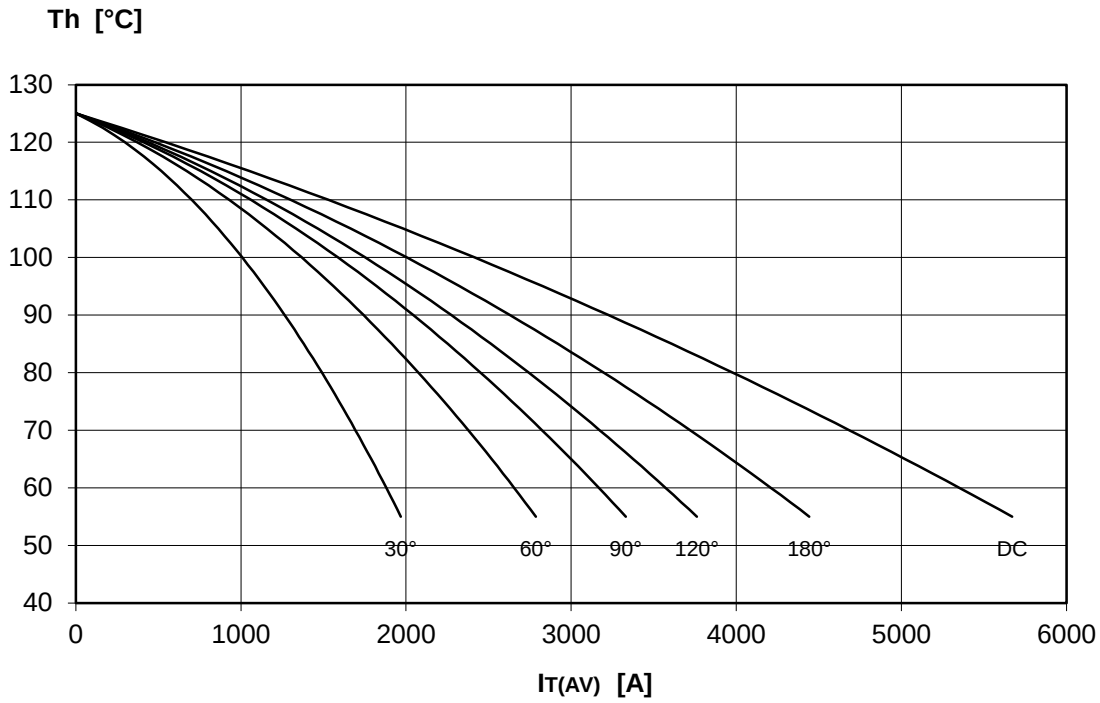
Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
V_{RRM}	Repetitive peak reverse voltage		125	1800	V
V_{RSM}	Non-repetitive peak reverse voltage		125	1900	V
V_{DRM}	Repetitive peak off-state voltage		125	1800	V
I_{RRM}	Repetitive peak reverse current	V=VRRM	125	150	mA
I_{DRM}	Repetitive peak off-state current	V=VDRM	125	150	mA
CONDUCTING					
$I_{T(AV)}$	Mean forward current	180° sin, 50 Hz, Th=55°C, double side cooled		4477	A
$I_{T(AV)}$	Mean forward current	180° sin, 50 Hz, Tc=85°C, double side cooled		3596	A
I_{TSM}	Surge forward current	Sine wave, 10 ms without reverse voltage	125	65	kA
I^2t	I^2t			21125 x 10^3	A^2s
V_T	On-state voltage	On-state current = 4000 A	25	1,25	V
$V_{T(TO)}$	Threshold voltage		125	0,99	V
r_T	On-state slope resistance		125	0,068	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	VD=67% VDRM; ITM=2000 A, non repetitive	125	400	A/µs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of VDRM	125	1000	V/µs
t_d	Gate controlled delay time, typical	VD=67%VDRM; IT=2000A, di/dt=10A/us tr=.0,5 µs	25	1	µs
t_q	Circuit commutated turn-off time, typical	dv/dt = 20 V/µs linear up to 80% VDRM		600	µs
Q_{rr}	Reverse recovery charge	di/dt = 10 A/µs, I= 2000 A	125	4650	µC
I_{rr}	Peak reverse recovery current	VR= 100 V		170	A
I_H	Holding current, typical	VD=5V, gate open circuit	25	1000	mA
GATE					
V_{GT}	Gate trigger voltage	VD=5V	25	3,00	V
I_{GT}	Gate trigger current	VD=5V	25	300	mA
V_{GD}	Non-trigger gate voltage, min.	VD=VDRM	125	0,25	V
V_{FGM}	Peak gate voltage (forward)				V
I_{FGM}	Peak gate current				A
V_{RGM}	Peak gate voltage (reverse)			5	V
P_{GM}	Peak gate power dissipation	Pulse width 100 µs		30	W
P_G	Average gate power dissipation			5	W
MOUNTING					
$R_{th(j-h)}$	Thermal impedance, DC	Junction to heatsink, double side cooled		9,0	°C/kW
$R_{th(c-h)}$	Thermal impedance	Case to heatsink, double side cooled		2	°C/kW
T_j	Operating junction temperature			-30 / 125	°C
F	Mounting force			36,0 / 44,0	kN
	Mass			550	g

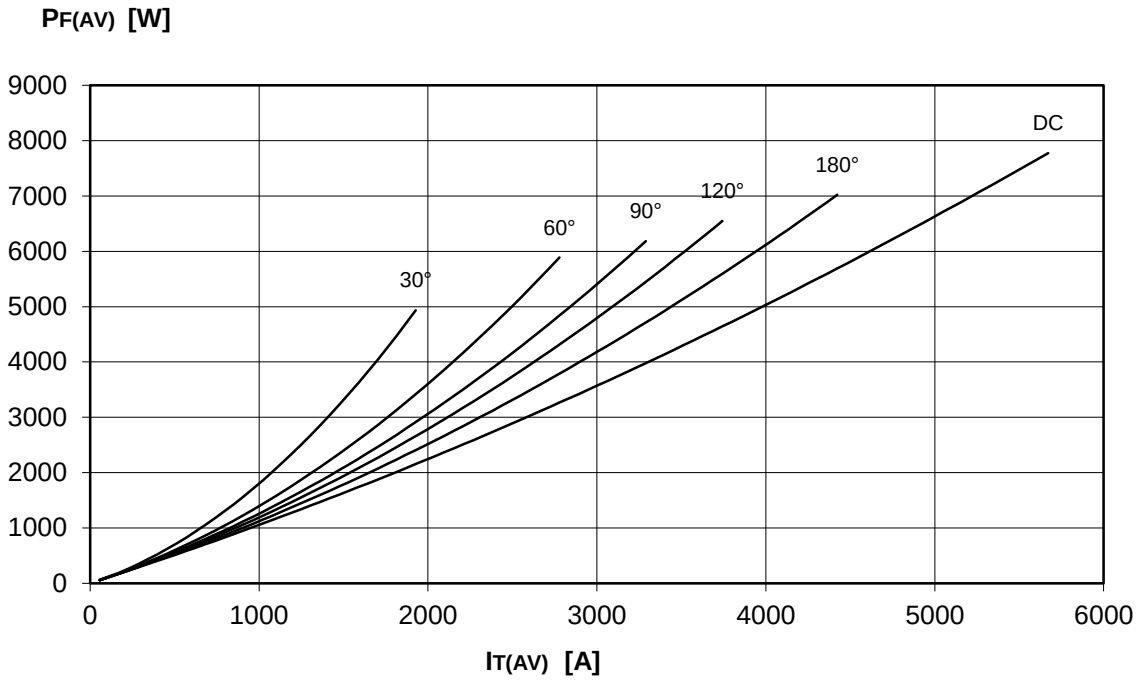
ORDERING INFORMATION : AT631LT S 18

standard specification — VRRM/100

DISSIPATION CHARACTERISTICS

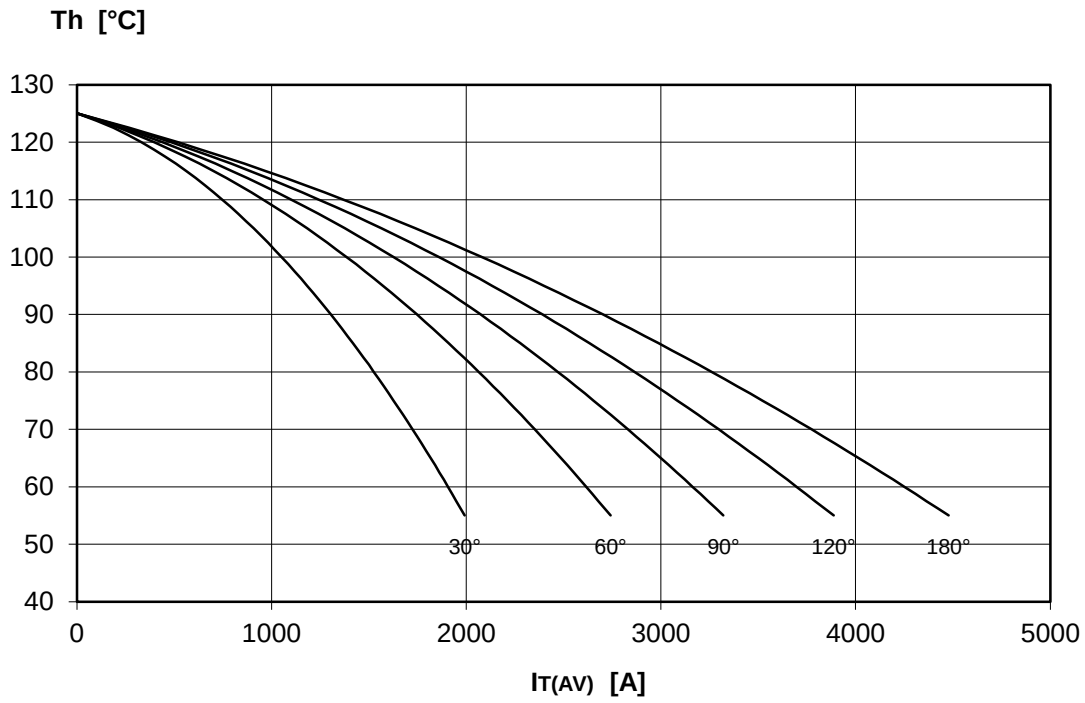
SQUARE WAVE

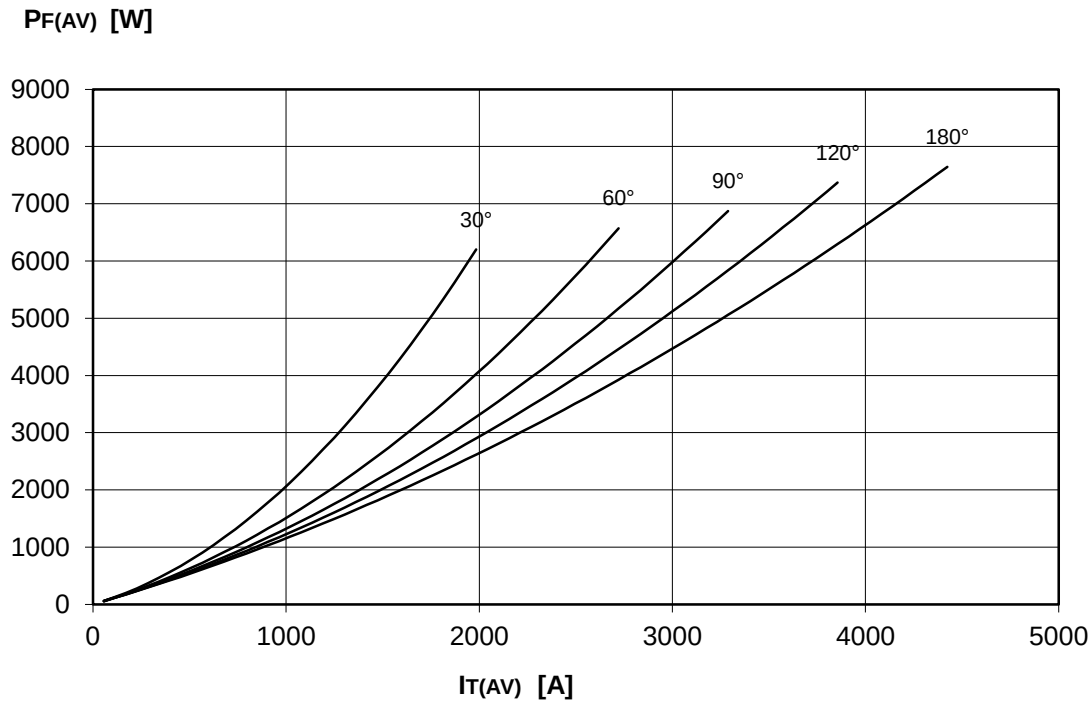




DISSIPATION CHARACTERISTICS

SINE WAVE





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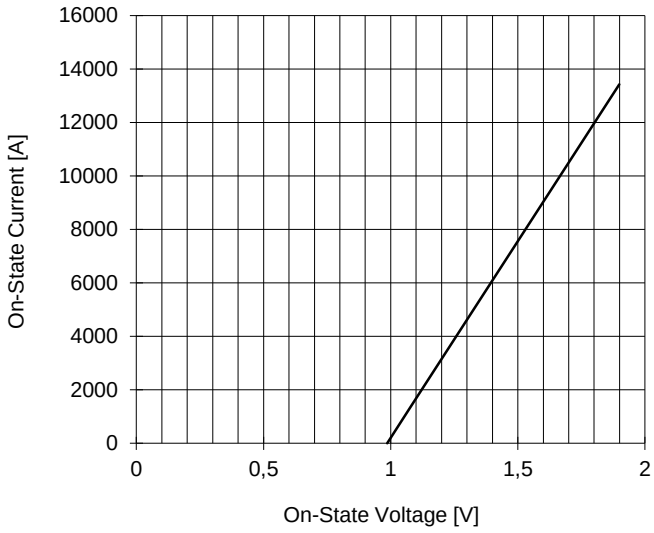
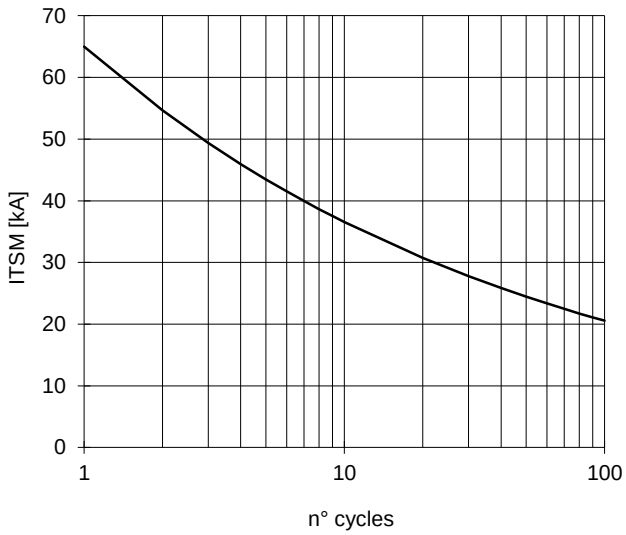
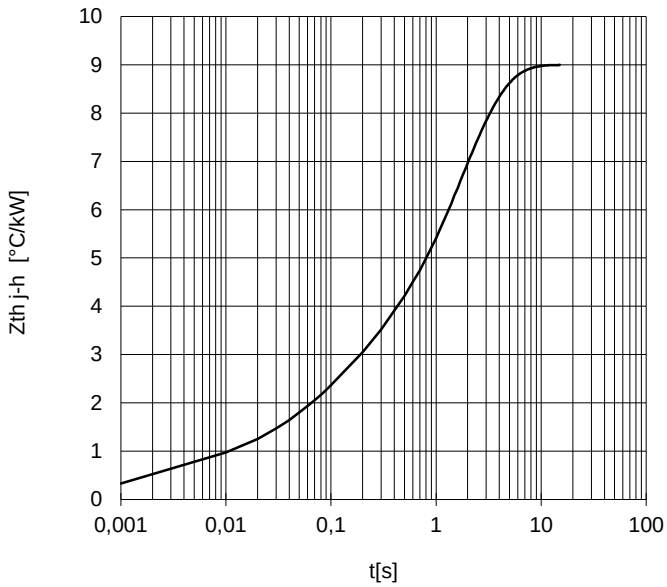
ON-STATE CHARACTERISTIC
Tj = 125 °C

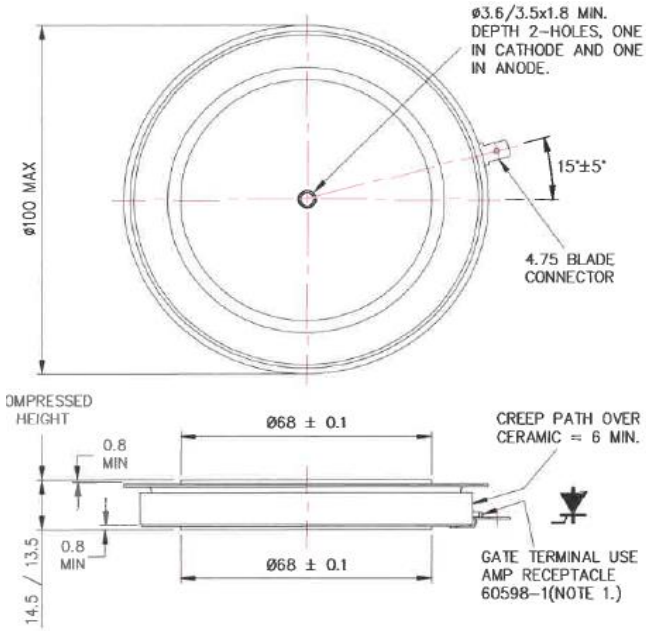


SURGE CHARACTERISTIC
Tj = 125 °C



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED





Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm.
In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.
If not stated otherwise the maximum value of ratings (simbols over shaded background) and characteristics is reported.

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